OIPE IAP61
MAR 03 2006
PATENT & TRADEMARK OFFICE

FIG. 1

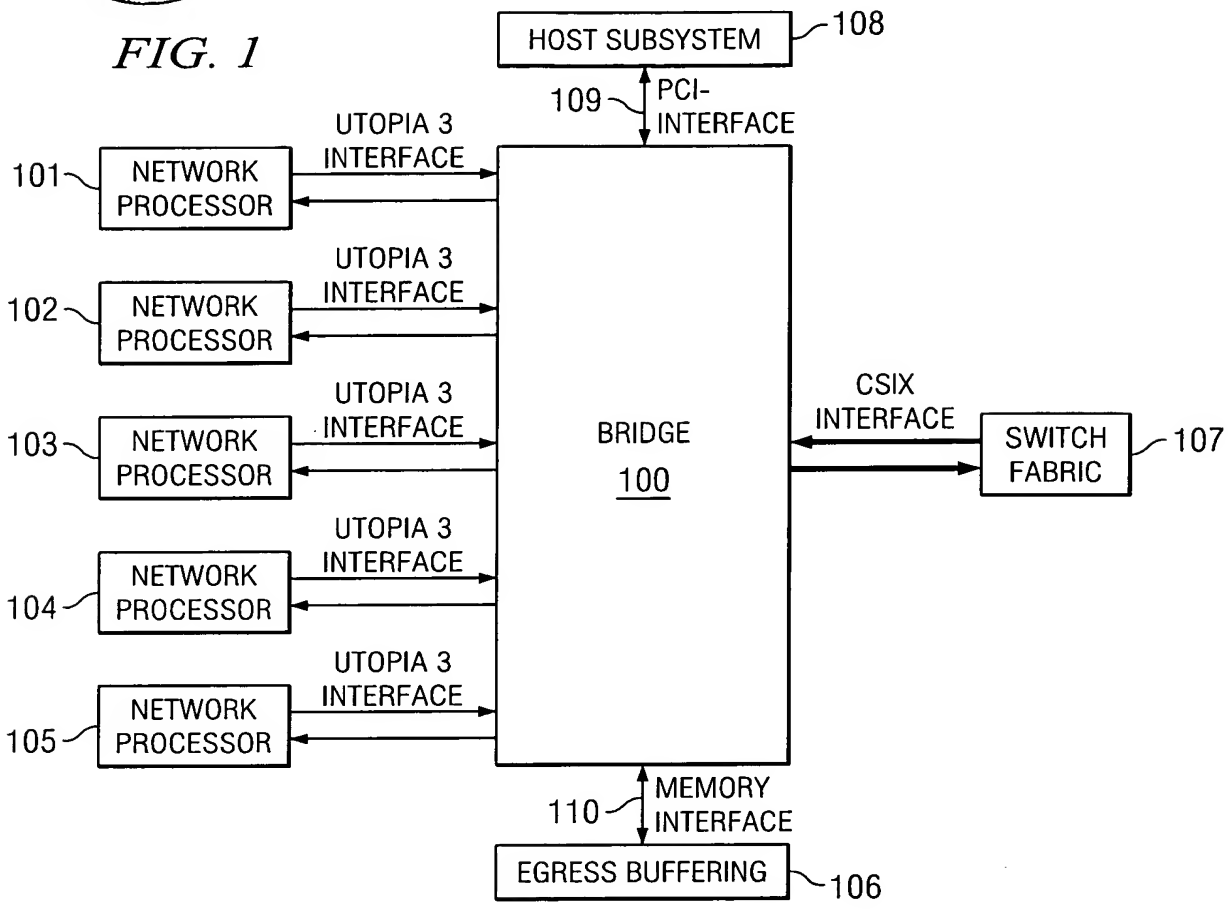
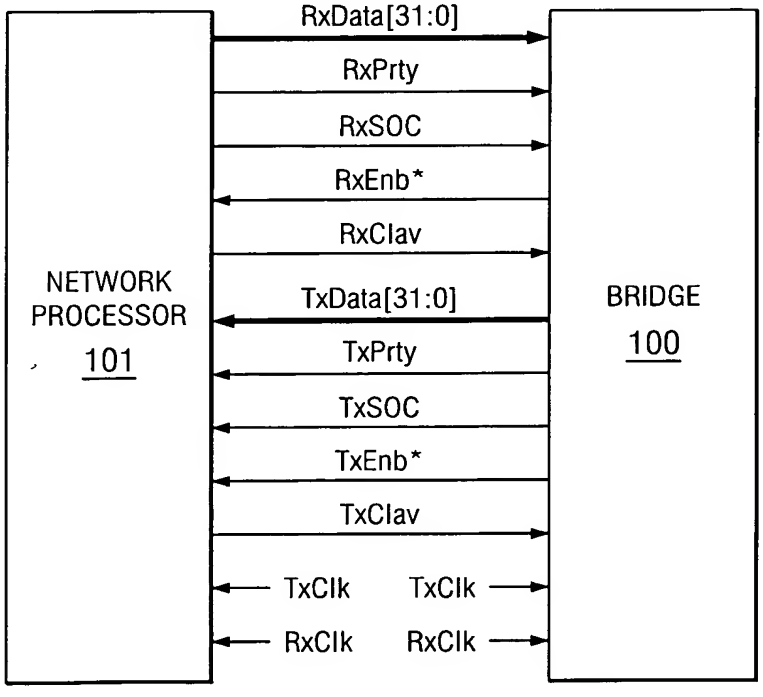


FIG. 2



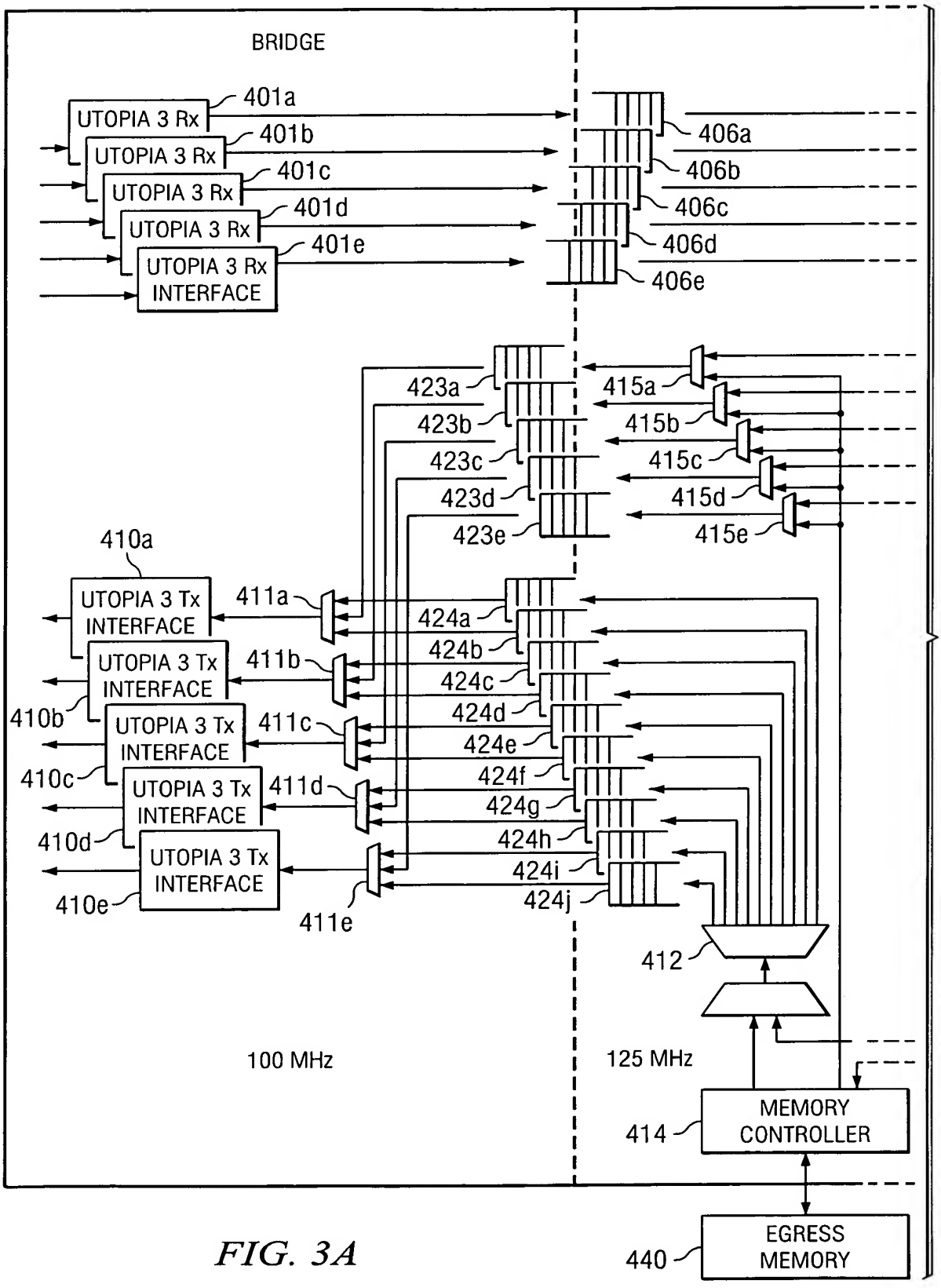

BRIDGE
UTOPIA 3 Rx
401a
UTOPIA 3 Rx
401b
UTOPIA 3 Rx
401c
UTOPIA 3 Rx
401d
UTOPIA 3 Rx
401e
UTOPIA 3 Rx INTERFACE
406a
406b
406c
406d
406e
423a
423b
423c
423d
423e
415a
415b
415c
415d
415e
410a
UTOPIA 3 Tx INTERFACE
411a
410b
UTOPIA 3 Tx INTERFACE
411b
410c
UTOPIA 3 Tx INTERFACE
411c
410d
UTOPIA 3 Tx INTERFACE
411d
410e
UTOPIA 3 Tx INTERFACE
411e
424a
424b
424c
424d
424e
424f
424g
424h
424i
424j
412
100 MHz
125 MHz
414
MEMORY CONTROLLER
440
EGRESS MEMORY
TO FIG. 3B

FIG. 3A

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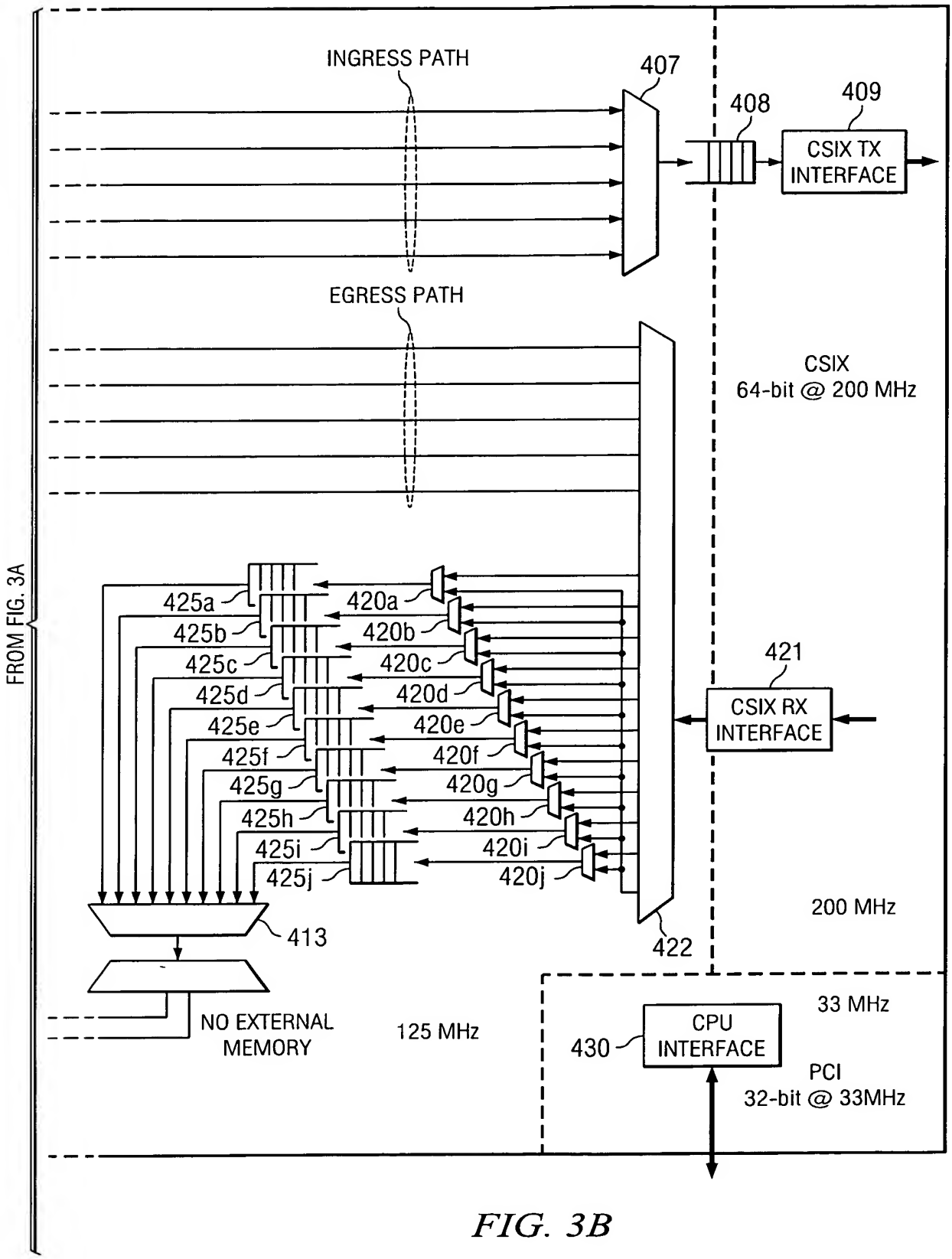

INGRESS PATH
407
408
409
CSIX TX INTERFACE
EGRESS PATH
CSIX
64-bit @ 200 MHz
FROM FIG. 3A
425a
425b
425c
425d
425e
425f
425g
425h
425i
425j
420a
420b
420c
420d
420e
420f
420g
420h
420i
420j
421
CSIX RX INTERFACE
413
422
200 MHz
NO EXTERNAL MEMORY
125 MHz
33 MHz
430
CPU INTERFACE
PCI
32-bit @ 33MHz

FIG. 3B

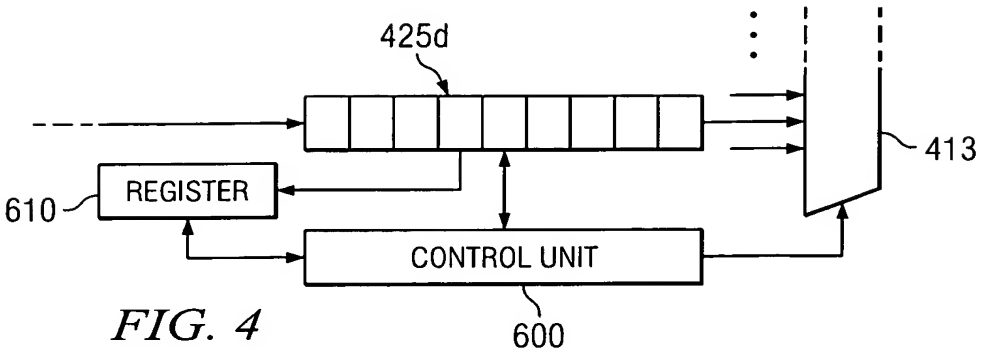


FIG. 4

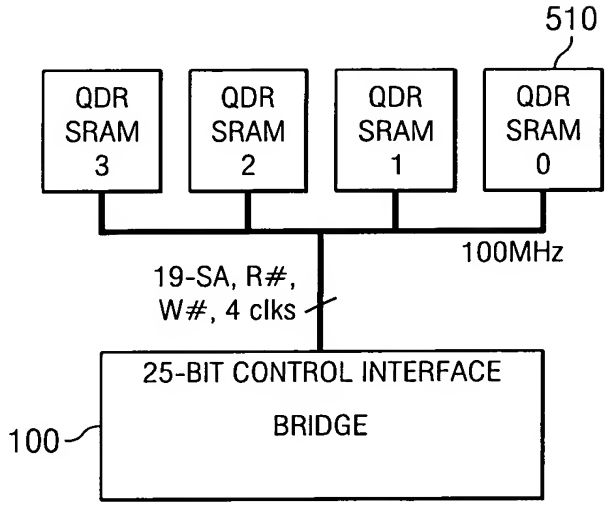


FIG. 5

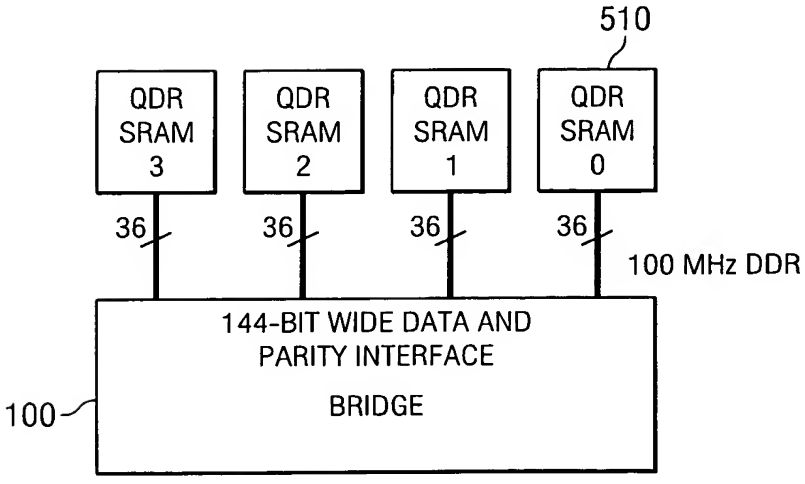
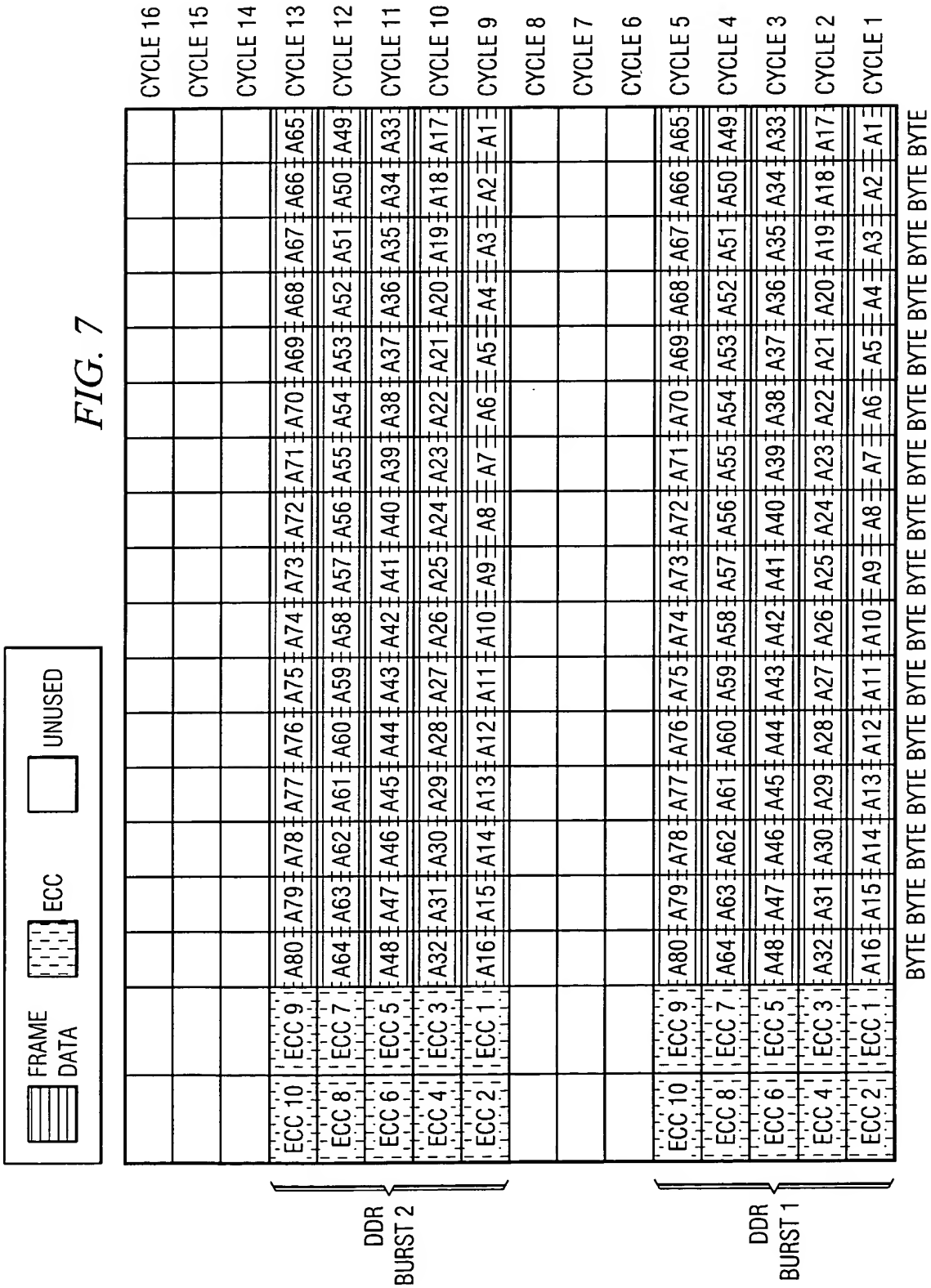


FIG. 6

FIG. 7


FRAME DATA
ECC
UNUSED
CYCLE 16
CYCLE 15
CYCLE 14
CYCLE 13
CYCLE 12
CYCLE 11
CYCLE 10
CYCLE 9
CYCLE 8
CYCLE 7
CYCLE 6
CYCLE 5
CYCLE 4
CYCLE 3
CYCLE 2
CYCLE 1
DDR BURST 2
DDR BURST 1
BYTE 16 BYTE 15 BYTE 14 BYTE 13 BYTE 12 BYTE 11 BYTE 10 BYTE 9 BYTE 8 BYTE 7 BYTE 6 BYTE 5 BYTE 4 BYTE 3 BYTE 2 BYTE 1

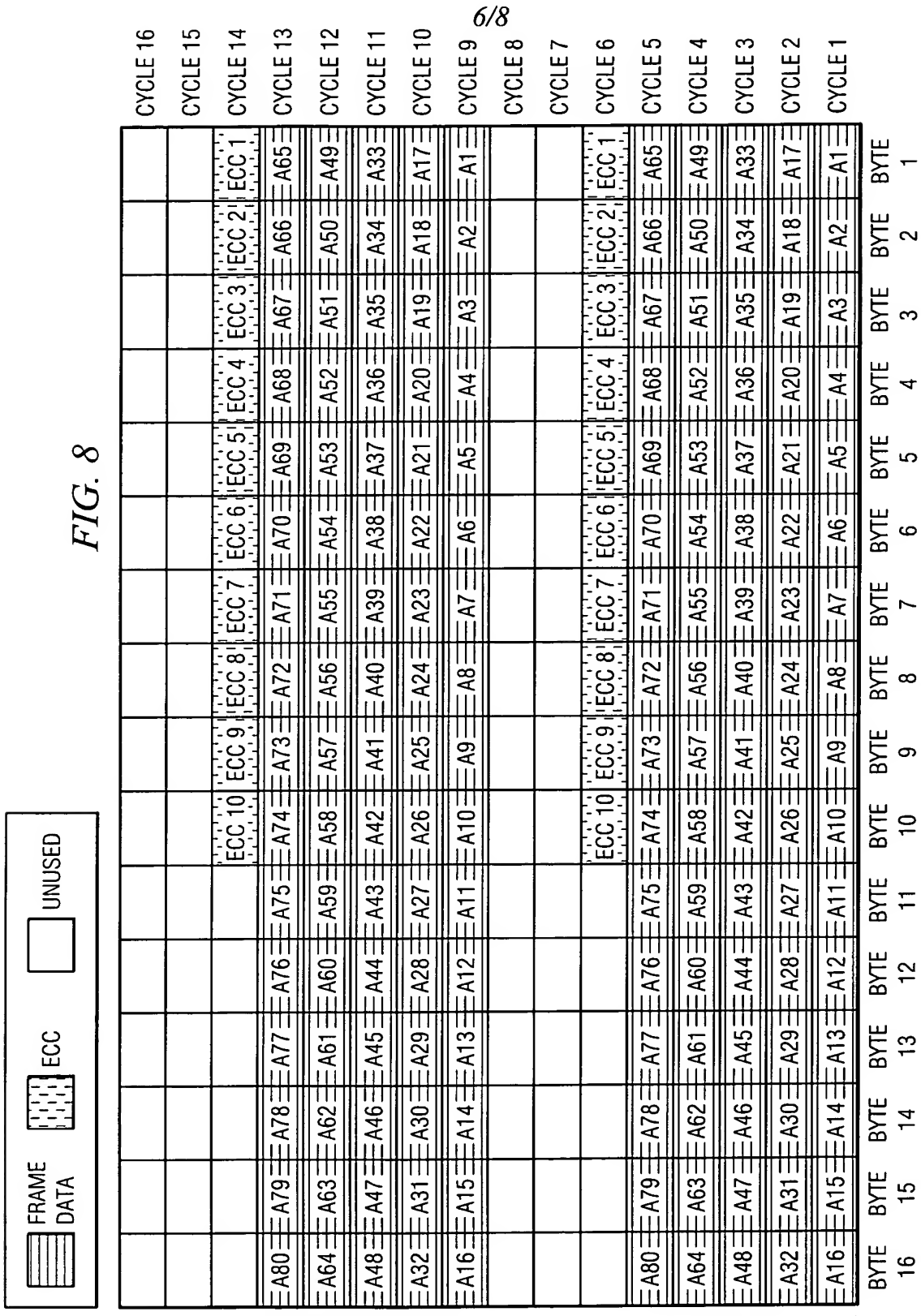
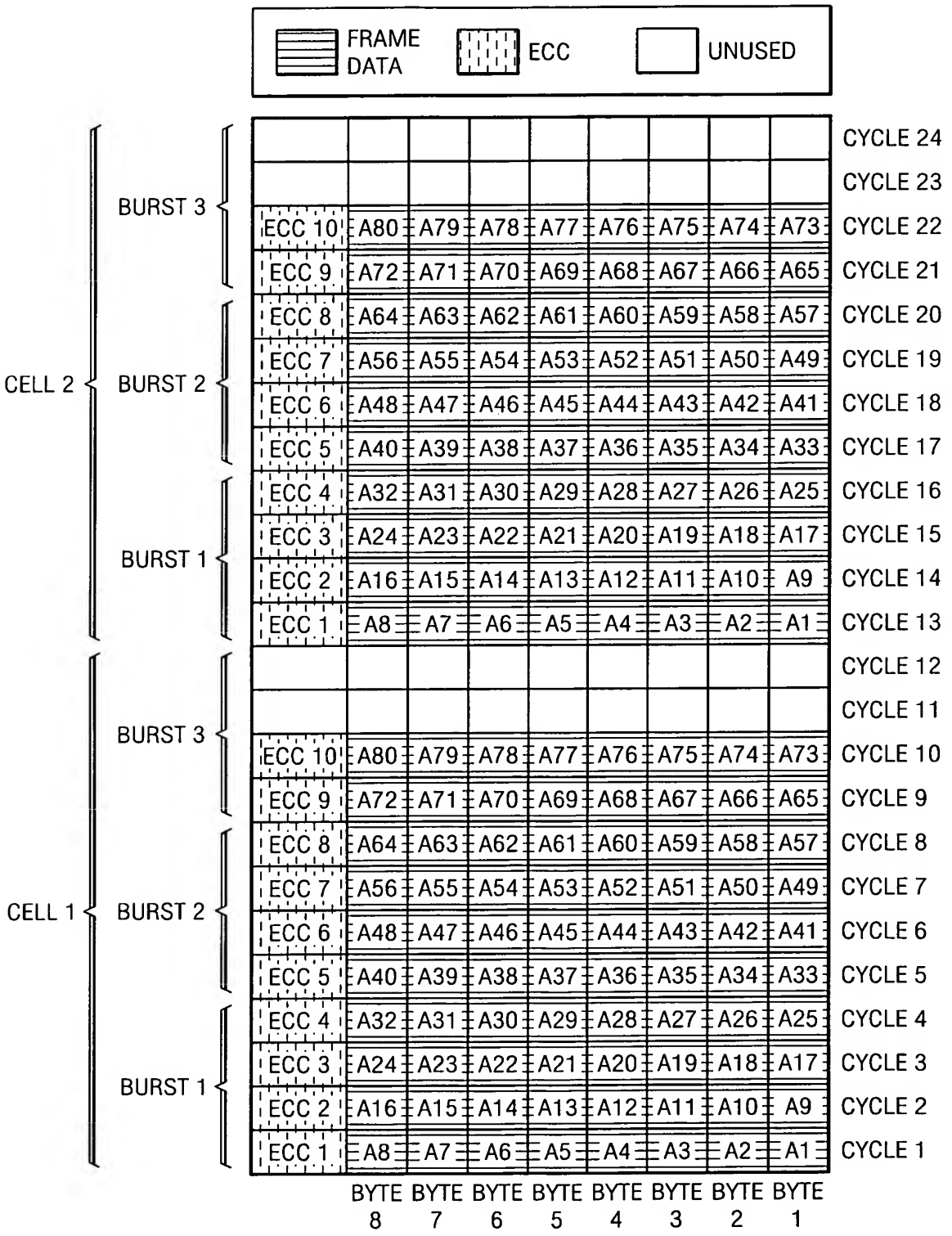

FRAME DATA
ECC
UNUSED
CYCLE 16
CYCLE 15
CYCLE 14
CYCLE 13
CYCLE 12
CYCLE 11
CYCLE 10
CYCLE 9
CYCLE 8
CYCLE 7
CYCLE 6
CYCLE 5
CYCLE 4
CYCLE 3
CYCLE 2
CYCLE 1
DDR BURST 2
DDR BURST 1
BYTE 16
BYTE 15
BYTE 14
BYTE 13
BYTE 12
BYTE 11
BYTE 10
BYTE 9
BYTE 8
BYTE 7
BYTE 6
BYTE 5
BYTE 4
BYTE 3
BYTE 2
BYTE 1

FIG. 8

FIG. 9


FRAME DATA
ECC
UNUSED
CELL 2
CELL 1
BURST 3
BURST 2
BURST 1
ECC 10 A80 A79 A78 A77 A76 A75 A74 A73 CYCLE 22
ECC 9 A72 A71 A70 A69 A68 A67 A66 A65 CYCLE 21
ECC 8 A64 A63 A62 A61 A60 A59 A58 A57 CYCLE 20
ECC 7 A56 A55 A54 A53 A52 A51 A50 A49 CYCLE 19
ECC 6 A48 A47 A46 A45 A44 A43 A42 A41 CYCLE 18
ECC 5 A40 A39 A38 A37 A36 A35 A34 A33 CYCLE 17
ECC 4 A32 A31 A30 A29 A28 A27 A26 A25 CYCLE 16
ECC 3 A24 A23 A22 A21 A20 A19 A18 A17 CYCLE 15
ECC 2 A16 A15 A14 A13 A12 A11 A10 A9 CYCLE 14
ECC 1 A8 A7 A6 A5 A4 A3 A2 A1 CYCLE 13
CYCLE 24
CYCLE 23
CYCLE 12
CYCLE 11
CYCLE 10
CYCLE 9
CYCLE 8
CYCLE 7
CYCLE 6
CYCLE 5
CYCLE 4
CYCLE 3
CYCLE 2
CYCLE 1
BYTE 8 BYTE 7 BYTE 6 BYTE 5 BYTE 4 BYTE 3 BYTE 2 BYTE 1

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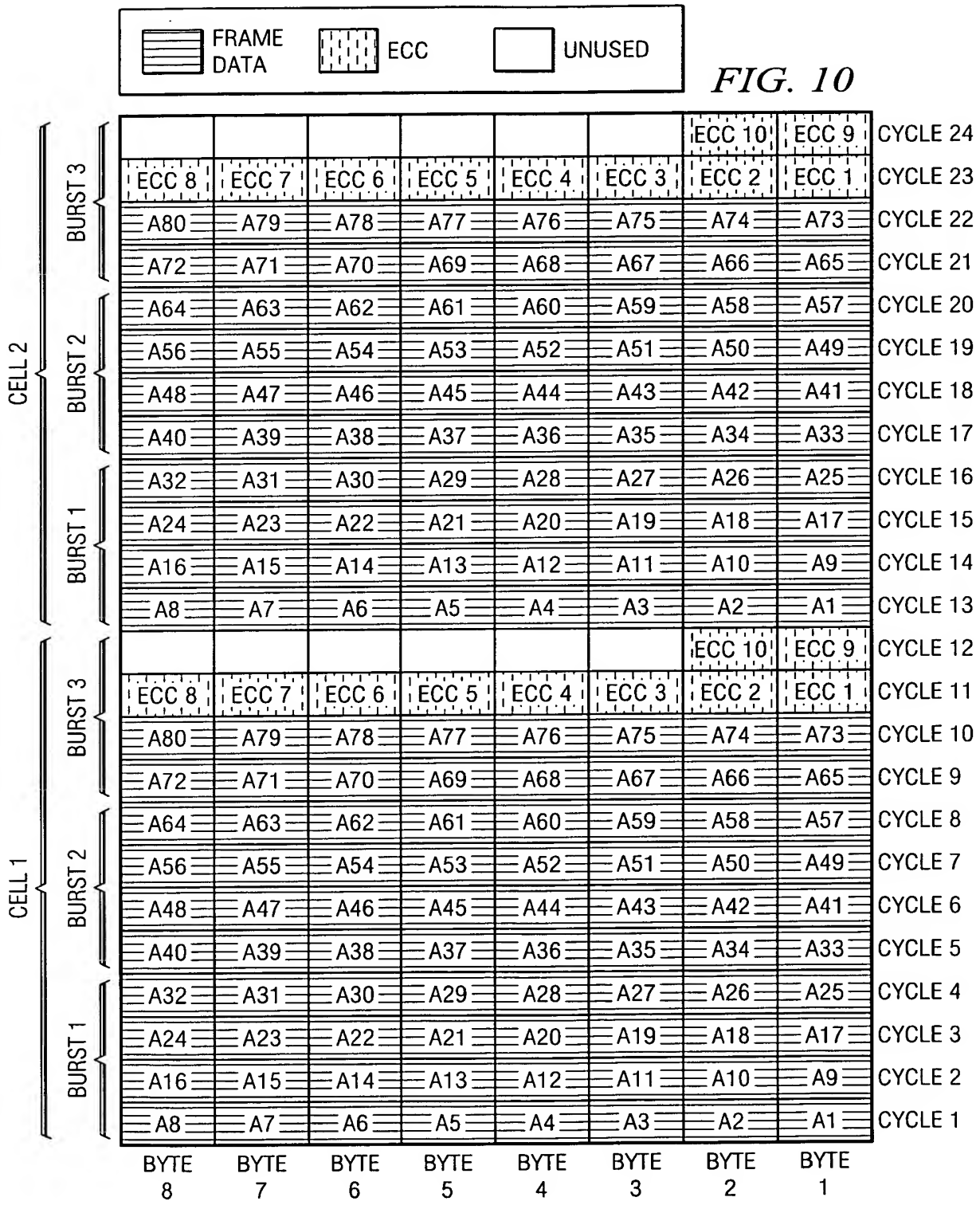
FRAME DATA
ECC
UNUSED
CELL 2
CELL 1
BURST 3
BURST 2
BURST 1
ECC 10 ECC 9 CYCLE 24
ECC 8 ECC 7 ECC 6 ECC 5 ECC 4 ECC 3 ECC 2 ECC 1 CYCLE 23
A80 A79 A78 A77 A76 A75 A74 A73 CYCLE 22
A72 A71 A70 A69 A68 A67 A66 A65 CYCLE 21
A64 A63 A62 A61 A60 A59 A58 A57 CYCLE 20
A56 A55 A54 A53 A52 A51 A50 A49 CYCLE 19
A48 A47 A46 A45 A44 A43 A42 A41 CYCLE 18
A40 A39 A38 A37 A36 A35 A34 A33 CYCLE 17
A32 A31 A30 A29 A28 A27 A26 A25 CYCLE 16
A24 A23 A22 A21 A20 A19 A18 A17 CYCLE 15
A16 A15 A14 A13 A12 A11 A10 A9 CYCLE 14
A8 A7 A6 A5 A4 A3 A2 A1 CYCLE 13
ECC 10 ECC 9 CYCLE 12
ECC 8 ECC 7 ECC 6 ECC 5 ECC 4 ECC 3 ECC 2 ECC 1 CYCLE 11
A80 A79 A78 A77 A76 A75 A74 A73 CYCLE 10
A72 A71 A70 A69 A68 A67 A66 A65 CYCLE 9
A64 A63 A62 A61 A60 A59 A58 A57 CYCLE 8
A56 A55 A54 A53 A52 A51 A50 A49 CYCLE 7
A48 A47 A46 A45 A44 A43 A42 A41 CYCLE 6
A40 A39 A38 A37 A36 A35 A34 A33 CYCLE 5
A32 A31 A30 A29 A28 A27 A26 A25 CYCLE 4
A24 A23 A22 A21 A20 A19 A18 A17 CYCLE 3
A16 A15 A14 A13 A12 A11 A10 A9 CYCLE 2
A8 A7 A6 A5 A4 A3 A2 A1 CYCLE 1
BYTE 8 BYTE 7 BYTE 6 BYTE 5 BYTE 4 BYTE 3 BYTE 2 BYTE 1

FIG. 10